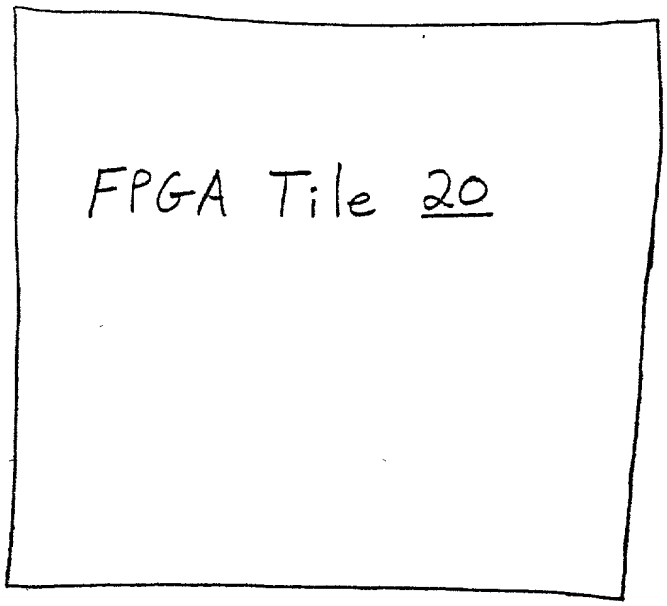

FIG. 1

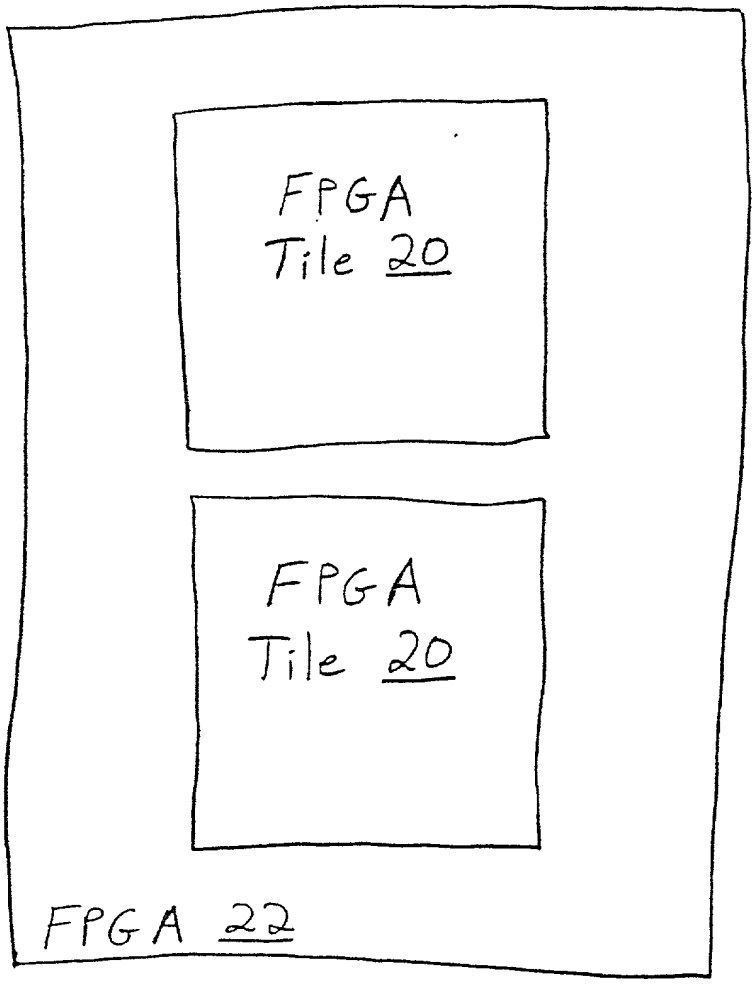

FIG. 2

ACT-318

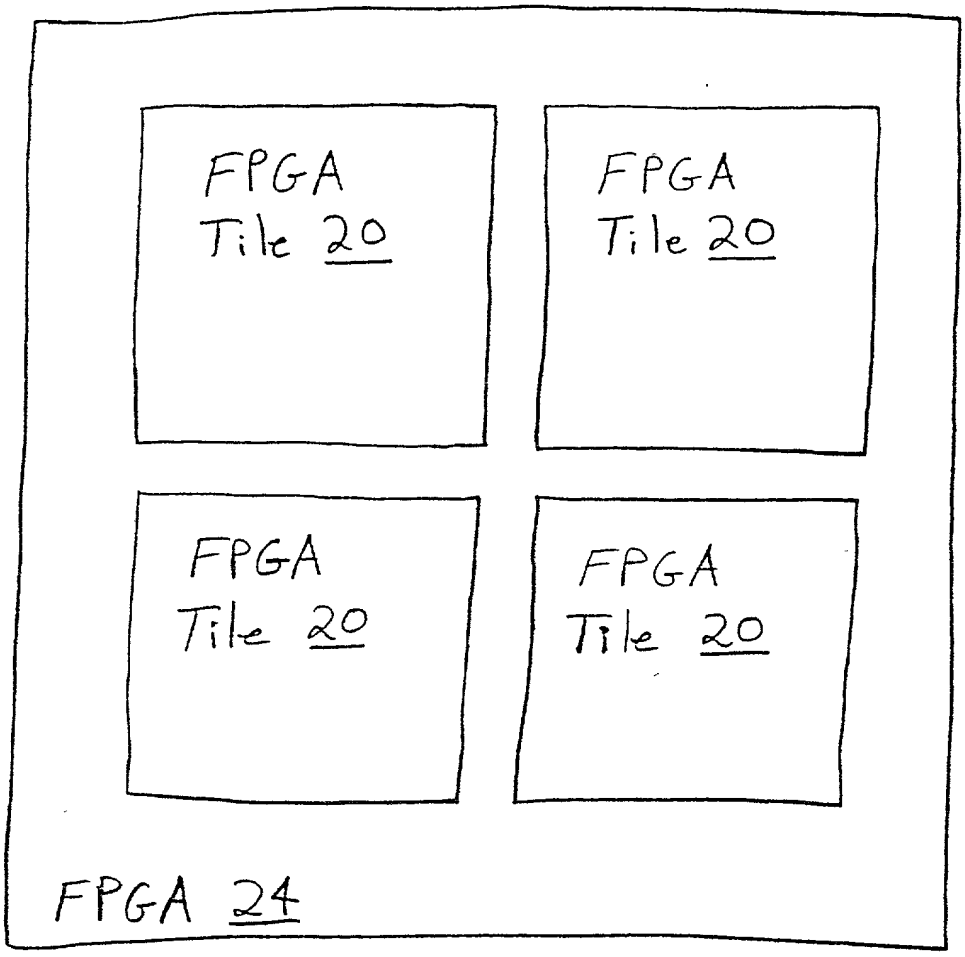

FIG. 3A

ACT-318

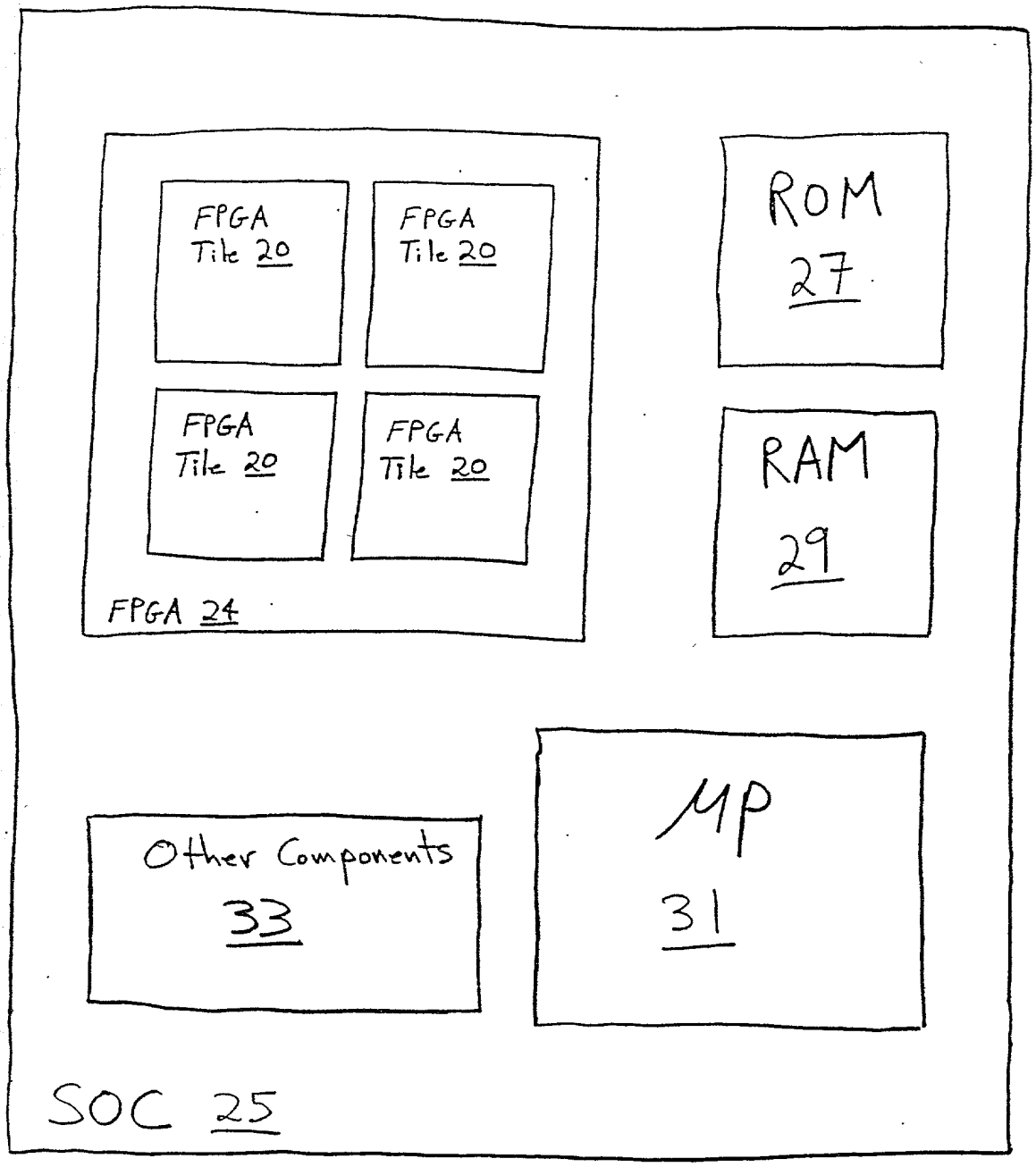

FIG. 3B

ACT-318

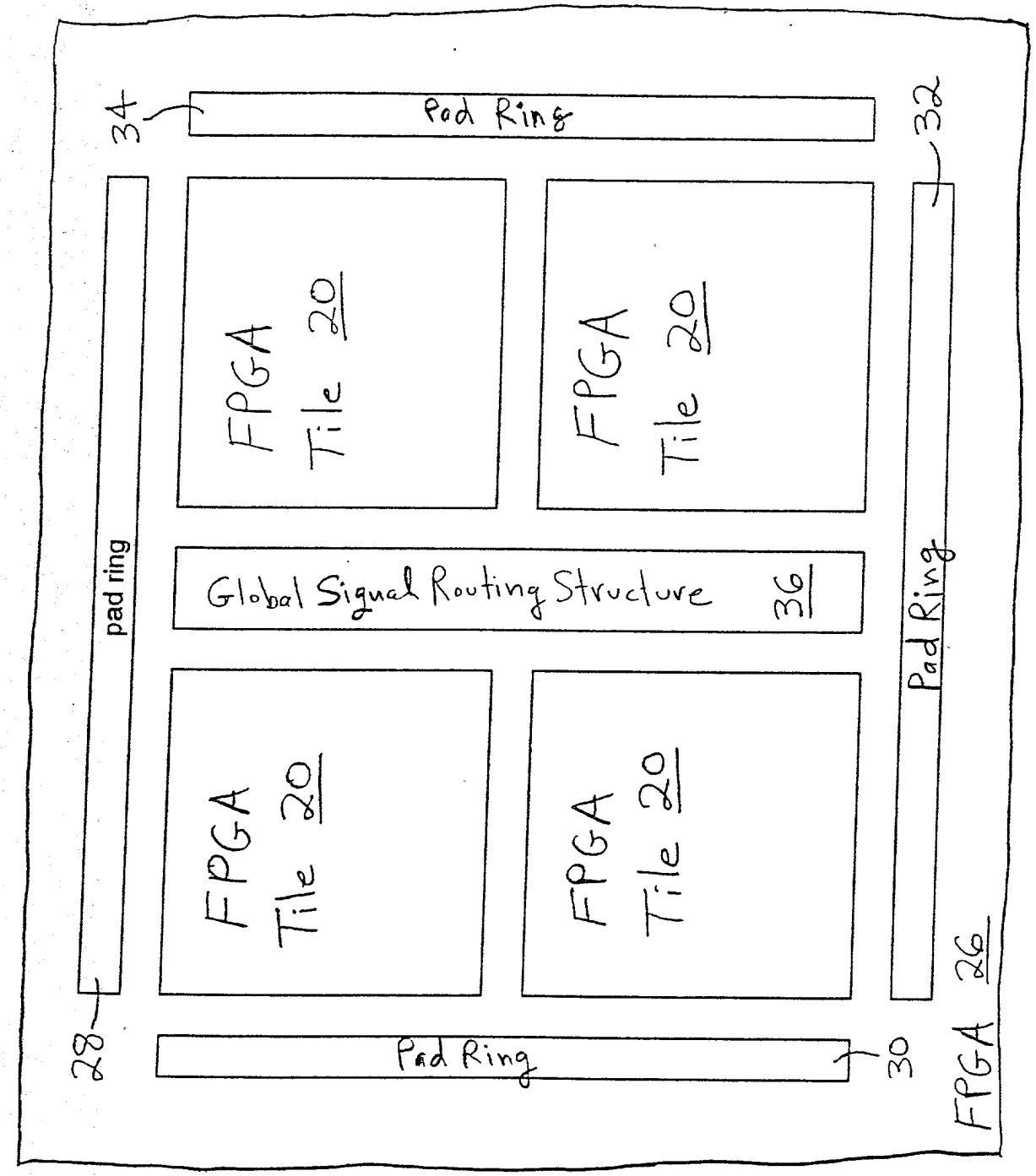
Pad Ring
34
32
FPGA Tile 20
FPGA Tile 20
pad ring
Global Signal Routing Structure 36
Pad Ring
FPGA Tile 20
FPGA Tile 20
28
Pad Ring
30
FPGA 26

FIG. 4

ACT-318

20

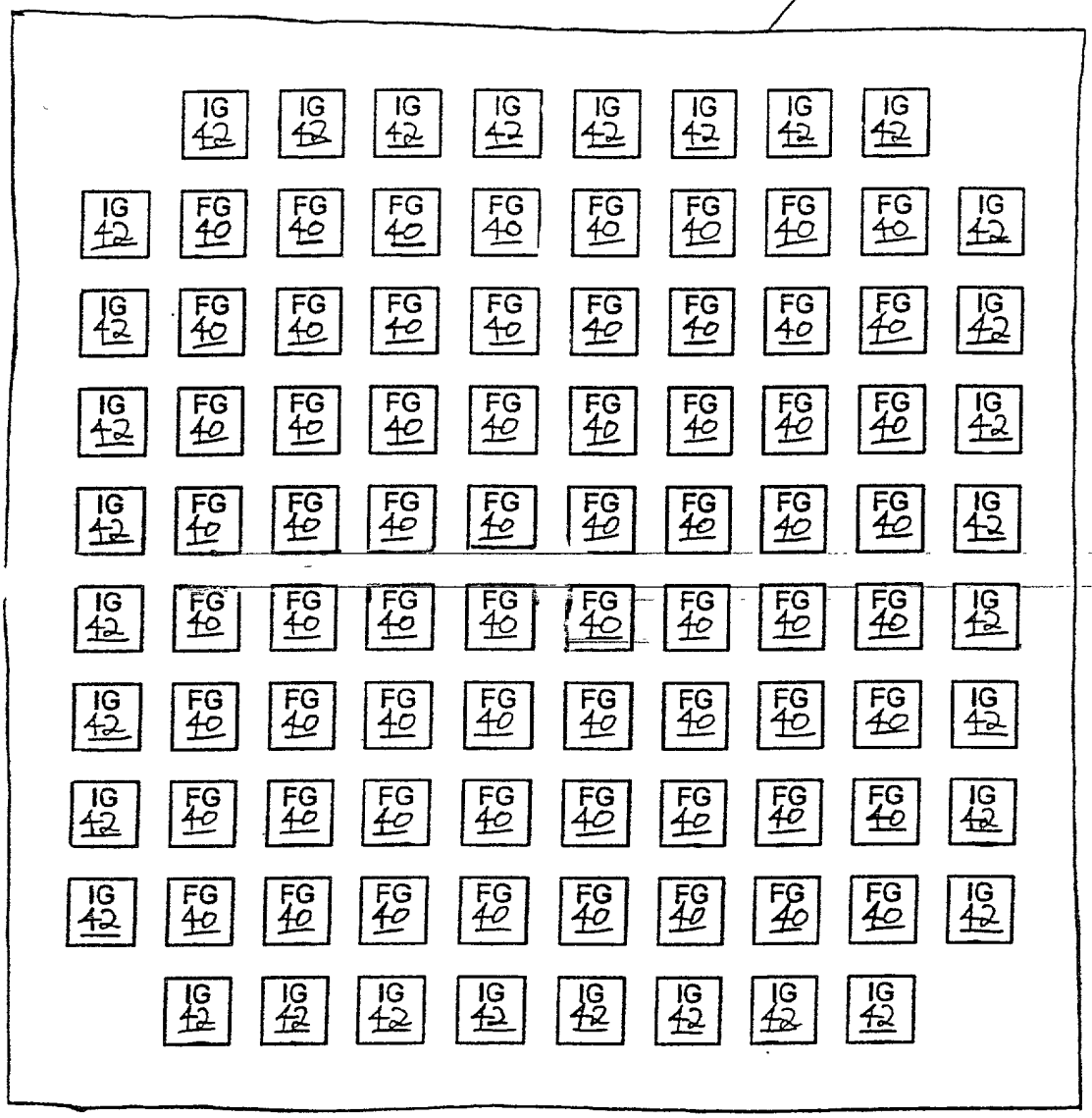

FIG. 5

ACT-318

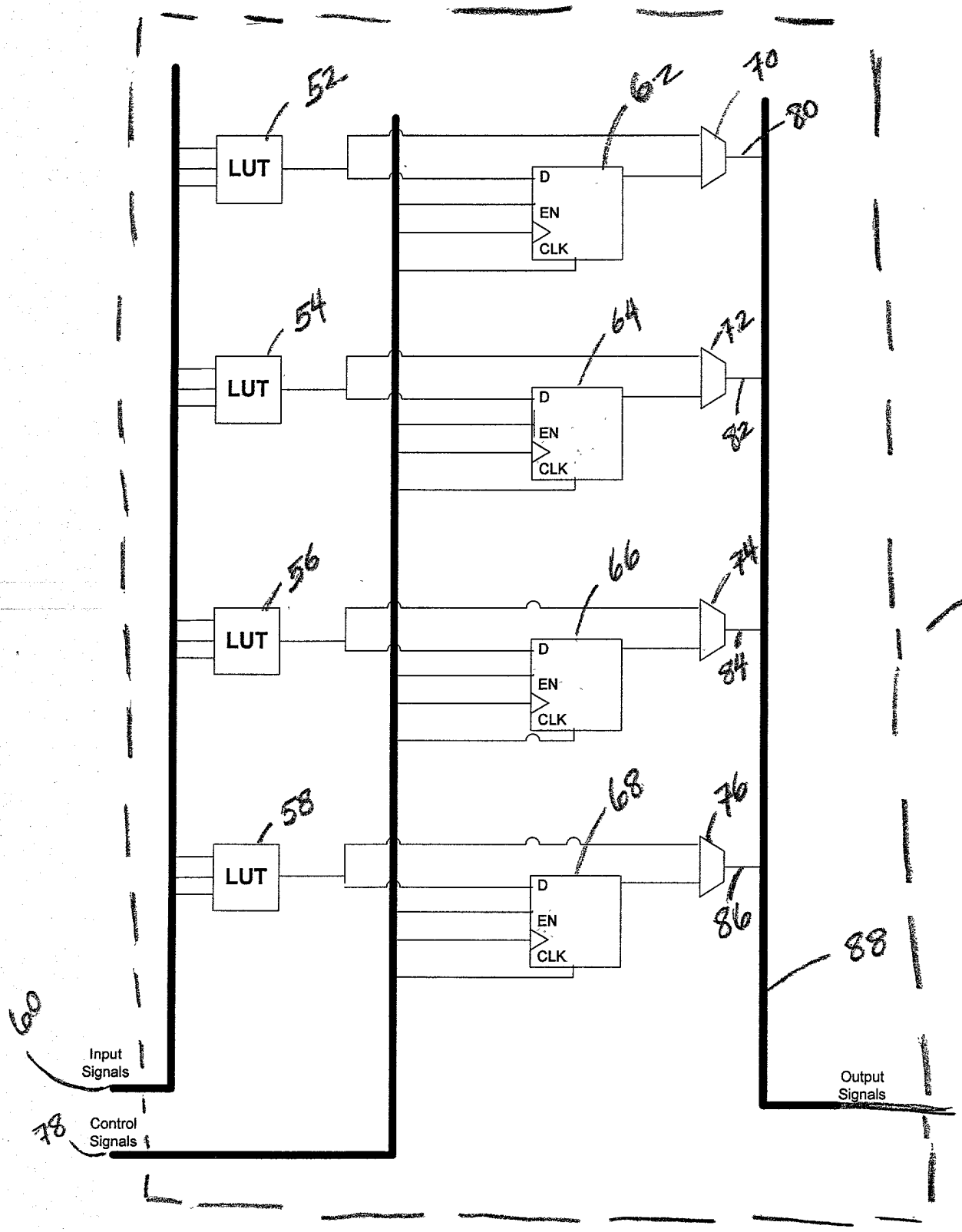
LUT
LUT
LUT
LUT
D
EN
CLK
52
54
56
58
62
64
66
68
70
72
74
76
80
82
84
86
88
40
60
Input Signals
78
Control Signals
Output Signals

FIG. 6

ACT-318

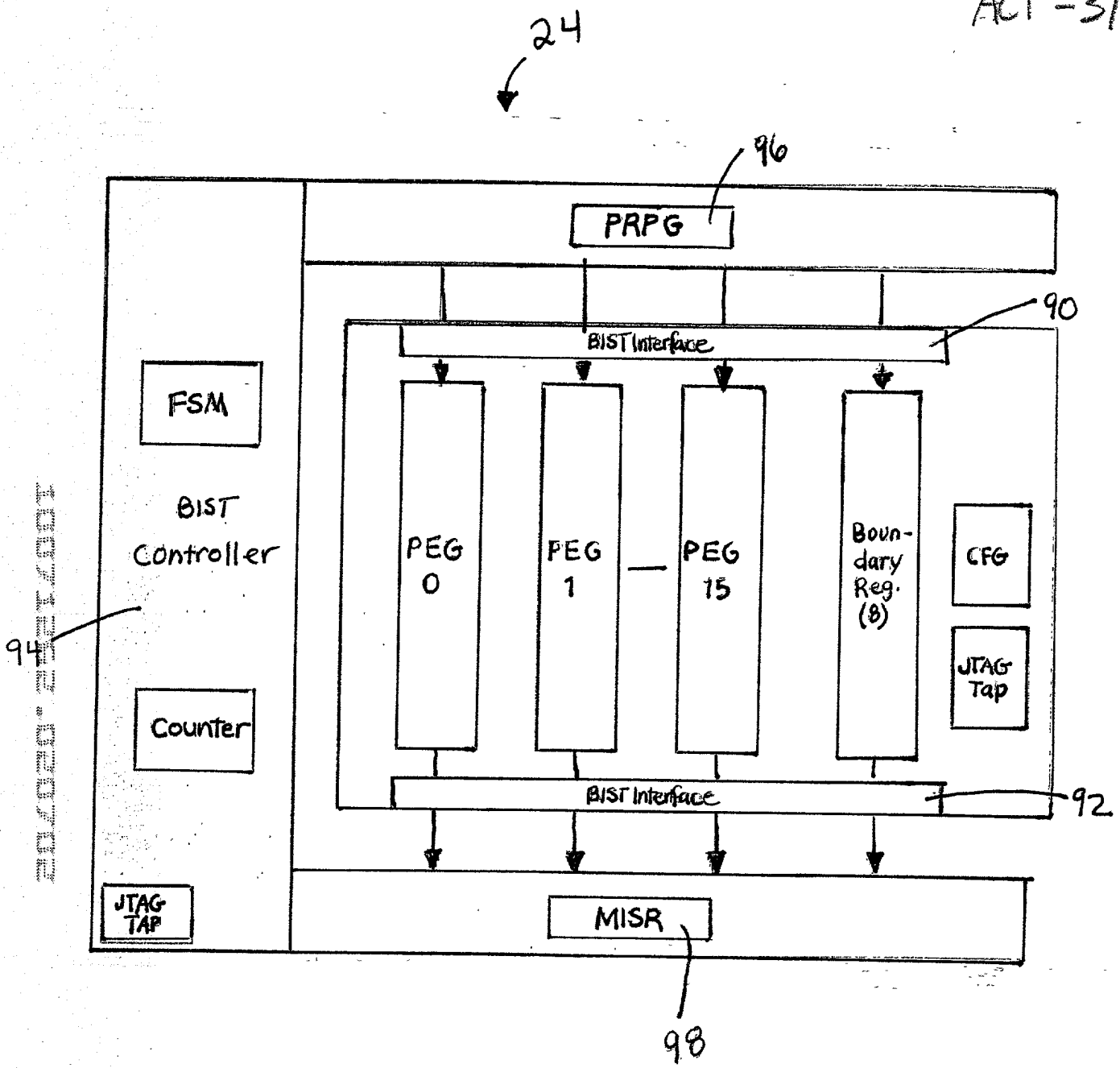
24
96
PRPG
90
BIST Interface
FSM
BIST Controller
94
PEG 0
PEG 1
PEG 15
Boun-dary Reg. (8)
CFG
JTAG Tap
Counter
BIST Interface
92
JTAG TAP
MISR
98

FIG. 7

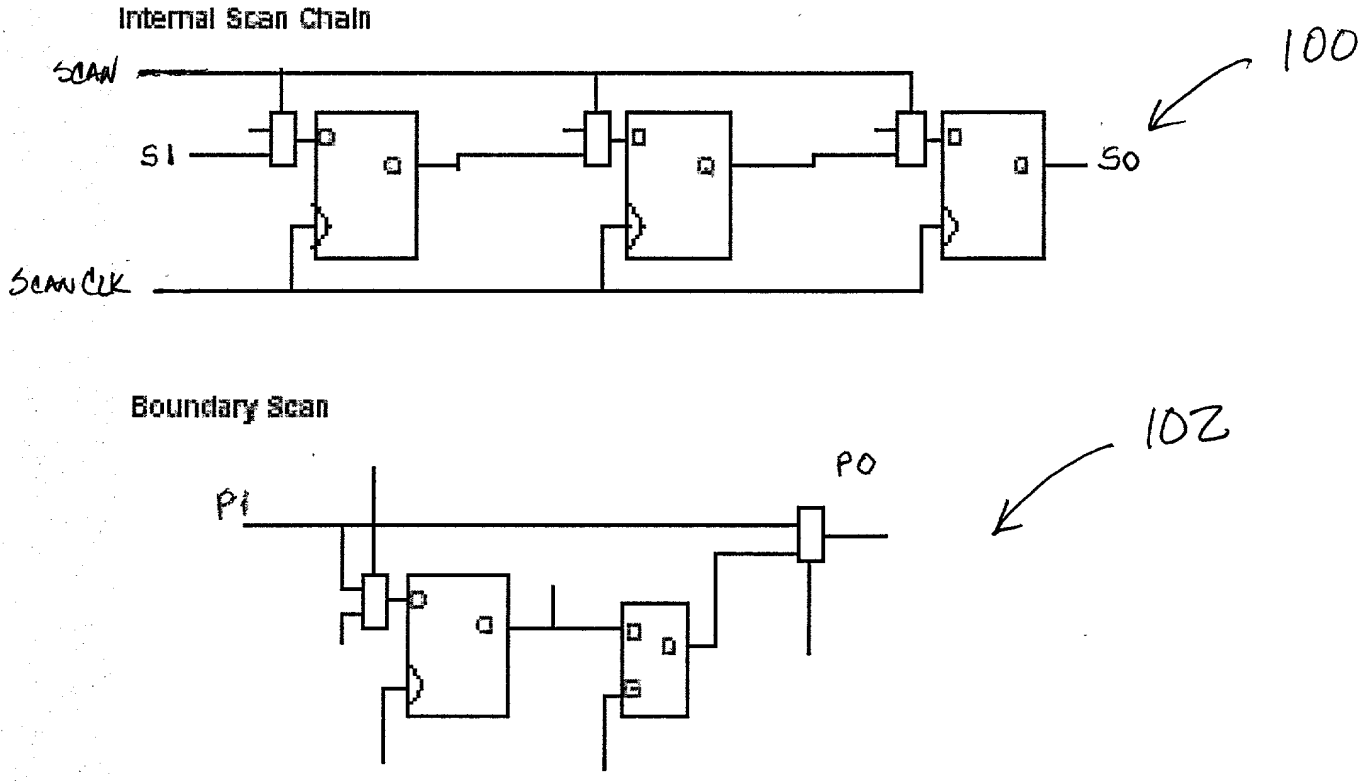
Internal Scan Chain
SCAN
SI
SCANCLK
SO
100
Boundary Scan
PI
PO
102

FIG. 8

ACT-318

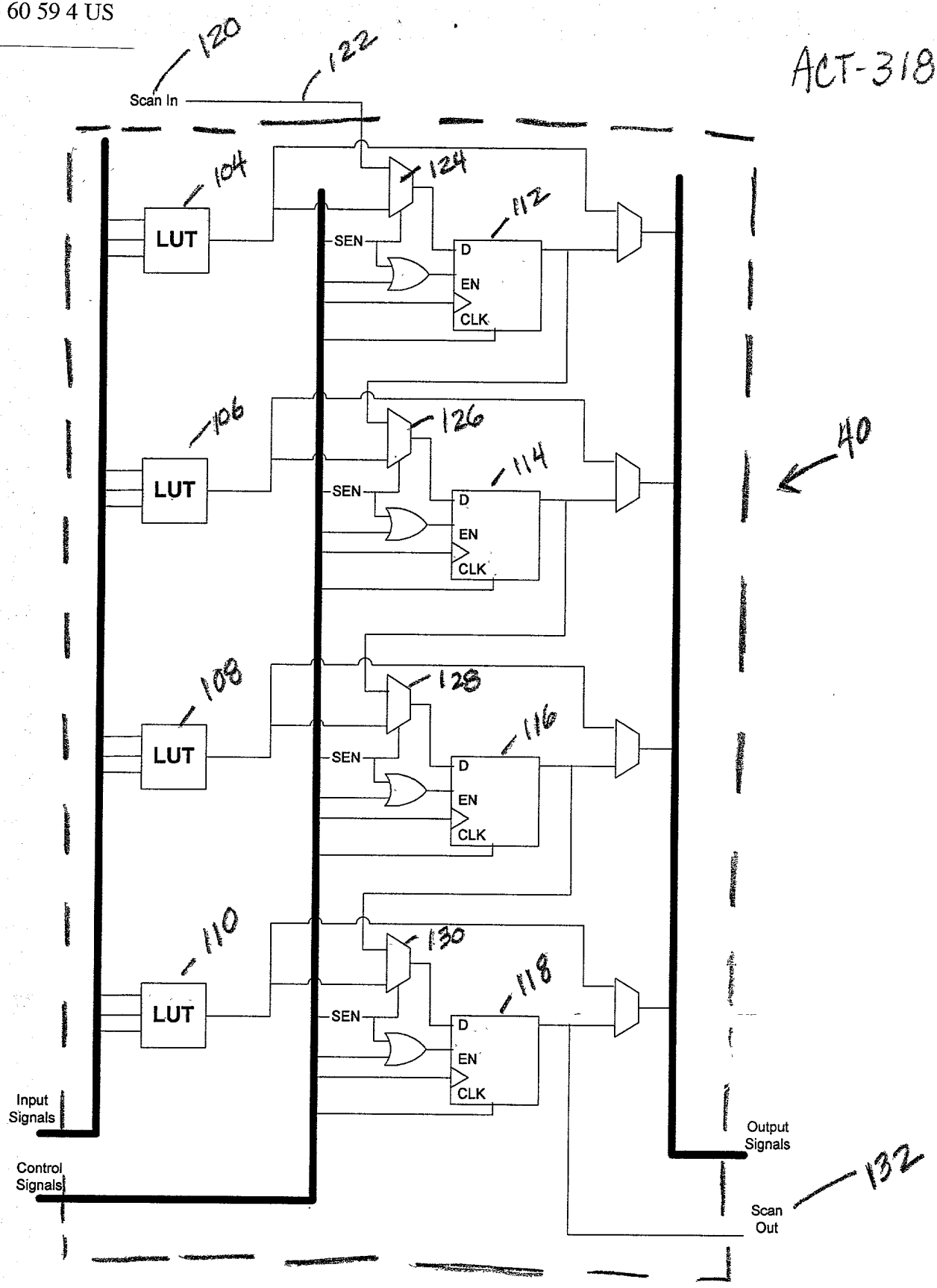
120
122
Scan In
104
LUT
124
SEN
112
D
EN
CLK
106
LUT
126
SEN
114
D
EN
CLK
40
108
LUT
128
SEN
116
D
EN
CLK
110
LUT
130
SEN
118
D
EN
CLK
Input Signals
Control Signals
Output Signals
Scan Out
132

FIG. 9

ACT-318

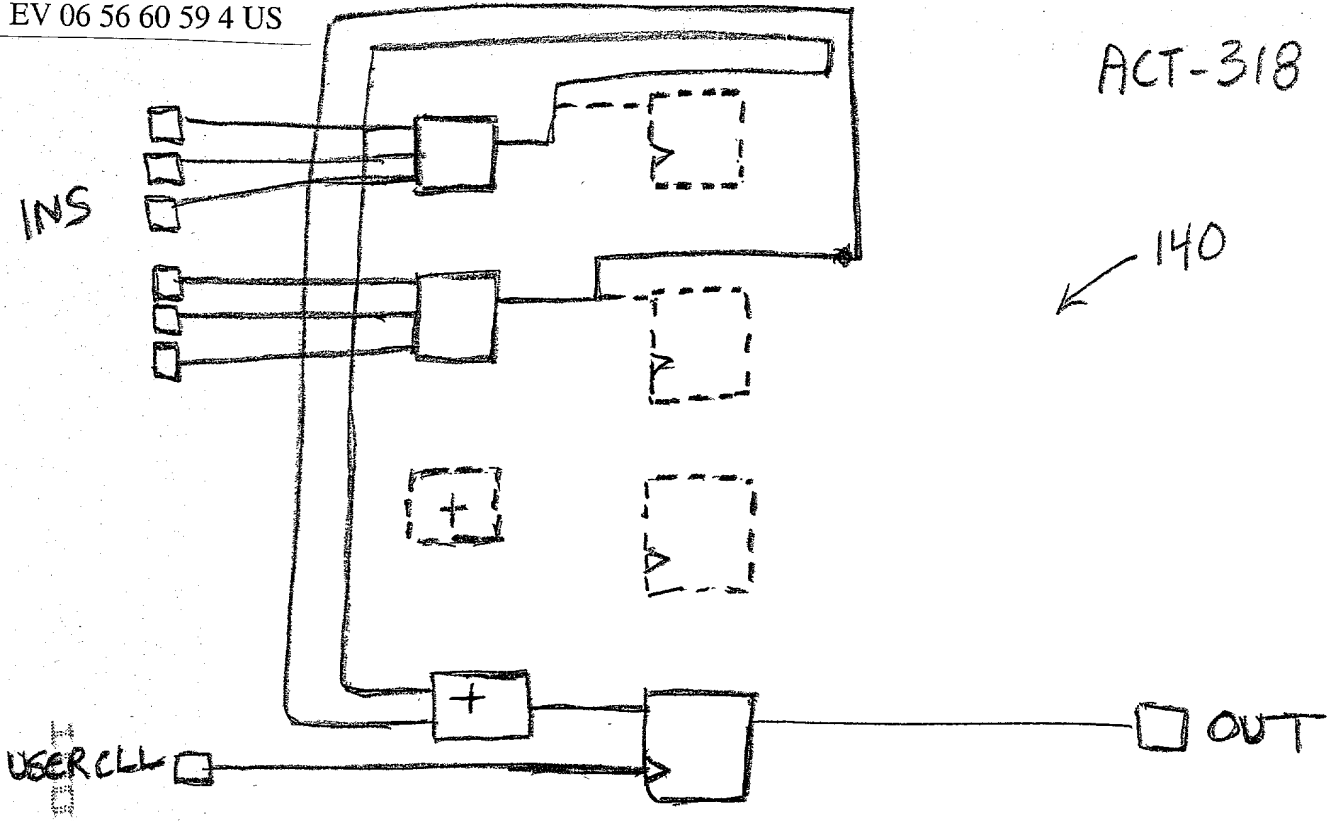

FIG.10A. USER LOGIC : Implemention of AND OR Circuit and register

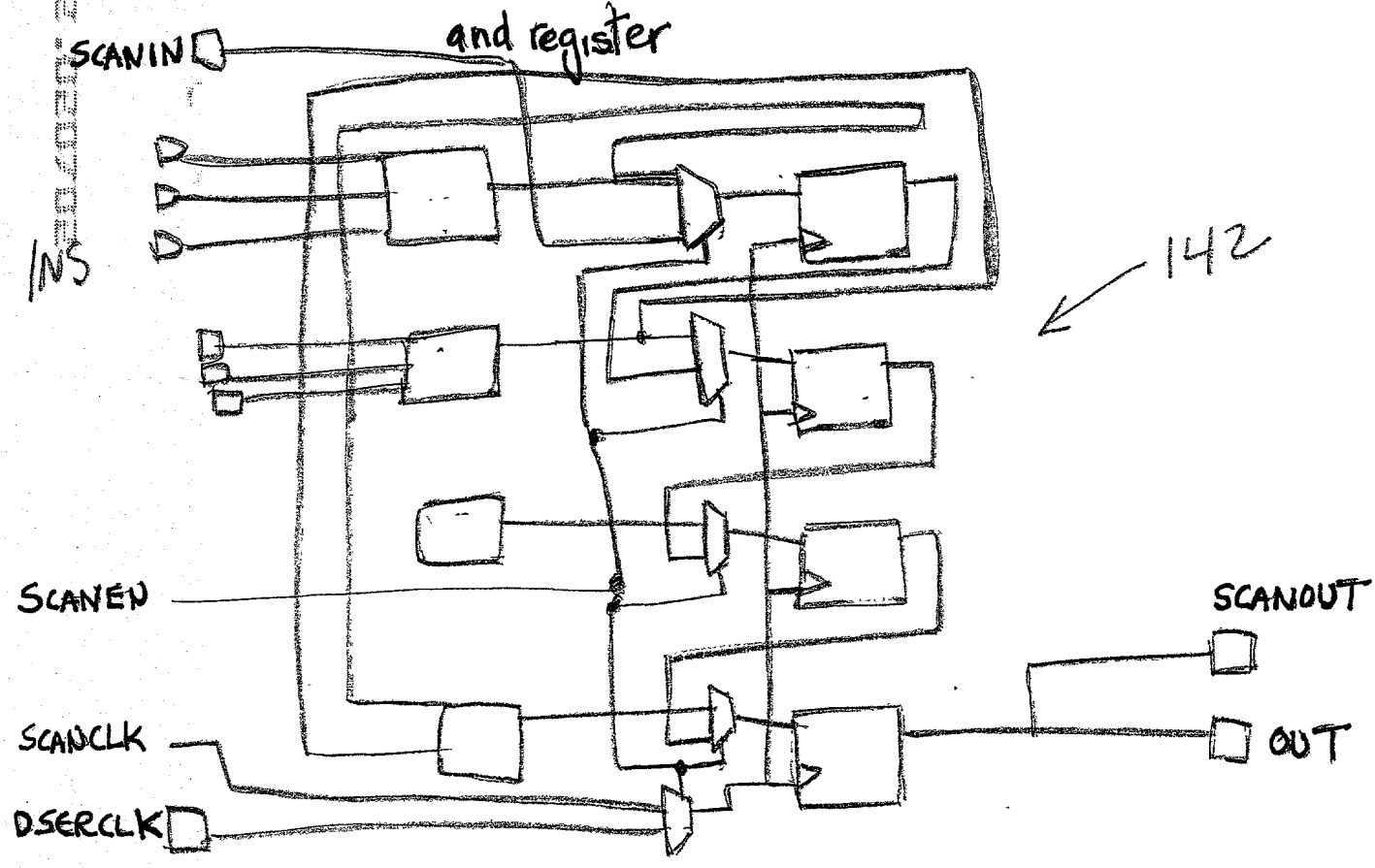

FIG.10B DSER Logic - With SCAN Superimposed

ACT-318

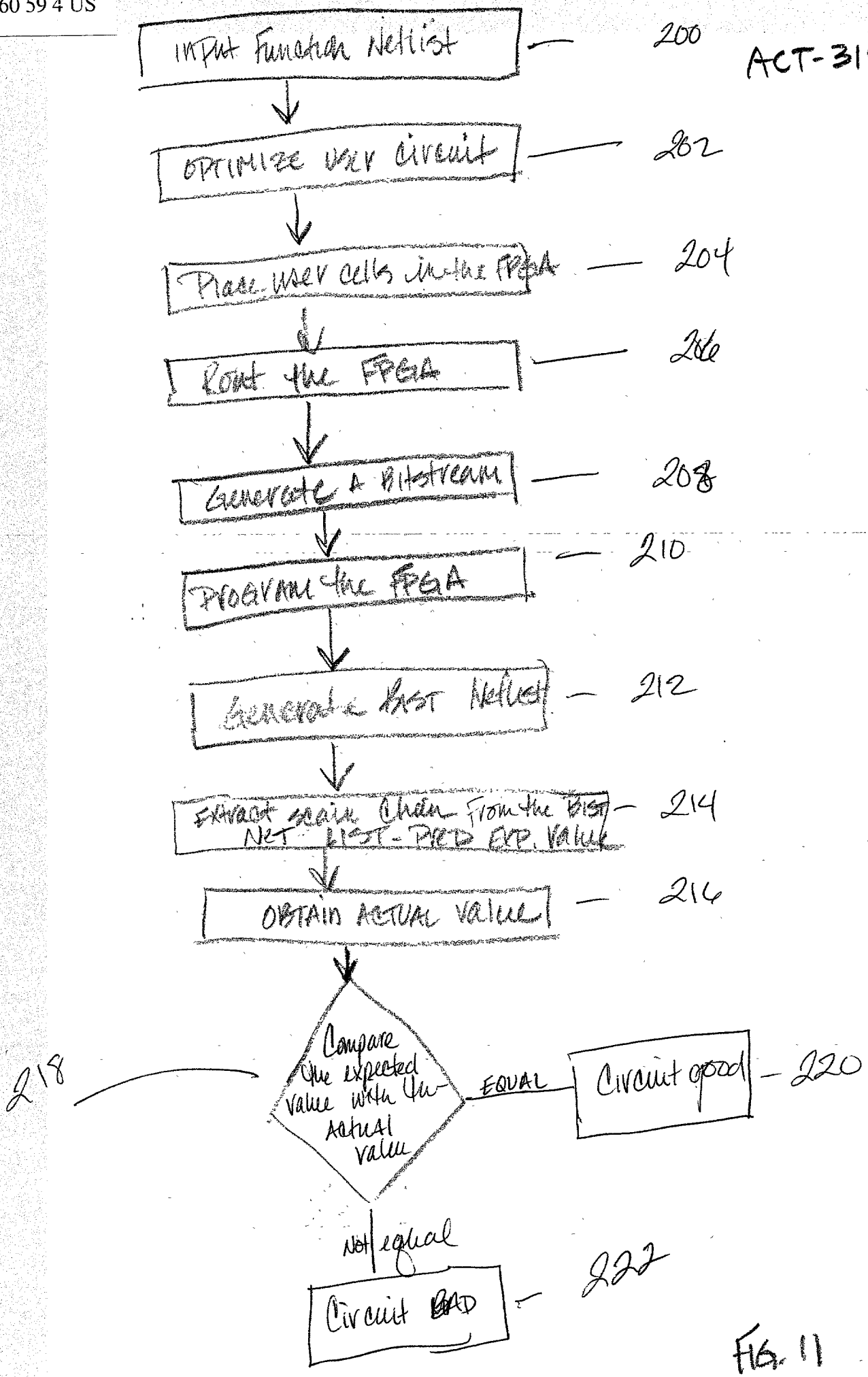

FIG. 11